Modeling of 24-Bit Noise Shaping ADC

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ABSTRACT

This paper presents a 9th order delta-sigma modulator with four-bit quantizer to achieve resolution of 24-bit at oversampling ration of 64. The modulator implements topology of cascade of integrators with multiple feedback (CIFB) for higher stability as loop filter order is increased and out-of-band gain (OBG) adjusted to 6. The signal transfer function is flat at low frequencies while noise transfer function shows noise shaping at high frequencies. Also, Noise transfer function with zero optimization technique is implemented considering further in band noise reduction. The integrators inside the loop filter optimized for higher performance. The operational amplifier DC gain, slew rate as well as unity gain bandwidth also studied. The limited DC gain causes reduction of resolution of the modulator. While the limited slew-rate also cause harmonic distortion in signal band. Therefore, it is important to study these performance parameters. As the order of the modulator is higher, the full scale of the modulator will be about 580 mV. Due to multiple feedback topology the signal swing inside the loop filter will be higher. Therefore, it demands operational amplifier with higher DC gain, higher slew-rate. Finally, the proposed 9th order 4-bit modulator can achieve signal to noise ratio of 148 dB with oversampling ratio of 64.

Keywords: Out-of-Band Gain, Full-scale input, Signal transfer function, Noise transfer function, Operational amplifier.

1. INTRODUCTION

Many of the practical parameters like temperature, pressure sensors or transducer output are very small. It is required to amplify these signals with very high and then required to digitized. It requires very high accuracy analog-to-digital converter (ADC). A 24-bit noise shaping modulator is modeled and simulated for moderate to smaller bandwidth application. The modulator performance parameters like full-scale and OBG varied to enhance the performance of the modulator. One of the fundamental restrictions of sensory systems is power consumption. With very small output signals provided by sensors, the power consumption of interface circuits processing small signals is quite significant. For given sampling capacitor size in high resolution SC systems with small input, large OSR is typically required to lower thermal noise level below system's accuracy requirement, which results in increased OTA amplifier power consumption. Even though technology scaling has lowered digital power in sensory systems, analogue front-end circuits, like as ADCs, have not profited from scaling in terms of power dissipation [1]-[3]. A 24-bit modulator design is proposed with chopping technique. The proposed design results high precision delta sigma ADC for low power, used for DC measurement, mainly in applications with high input impedance. The design uses the 3rd order modulator with signle-bit quantizer. The design starts from modeling the design and finding the coefficient and getting an estimate of the performance of the modulator. The

estimated performance of the modulator will be used as initial value that may degrade and result in much lower performance. To reduce an input dependent residual offset which is generated through a clock feed through, an adjustable chopping mechanism is also provided. Furthermore, it increases first integrator's noise performance. The delay generation for the chopping techniques to adjust the delay cell timing. The digital control logic will generate the logic for these delay cells. This chip is designed in 65nm technology, and its area is 1.17mm^2. A 3.3 volt is applied as a power supply and total power dissipation is 860 microwatts. ADC get a 20-bit resolution, 0.6 micro volt offset and 10 ppm INL. It also overcomes mismatch in 1st integrator and offset which is caused by clock feedthrough. To overcome chopping spikes a delay cell is applied. At the same time, to remove mismatches of integrator one more chopper is applied [4]. For applications of a battery powered sensor, 20 bit incremental analog to digital converter is presented. It's based on low-power zoom ADC architecture that uses a course 6 bit SAR conversion followed by fine 15 bit delta sigma conversion. To get more PVT tolerance and gain ADC uses integrators which on basis of cascoded dynamic inverters to improve its energy efficiency even more. To accomplish both low offset and good linearity, dynamic error correction techniques including as chopping, auto-zeroing and DEM are used. This ADC get 20 bit resolution, 1 micro volt offset and 6 ppm INL at conversion time which is 40ms.The power supply voltage is 1.8 volt and drawing current is 3.5 micro ampere. This corresponds to state of the art FoM of 182.7 dB. 160nm CMOS technology is used and chip area is 0.35mm^2 [5]. Another work describes a second-order incremental converter based on 2nd order delta sigma modulator. The approach employs a 3 bit DAC with inherent linearity, ideal integrator reset, and unique technique based on single or double chopping to provide effective offset cancellation. The circuit, designed in mixed 0.18-0.6 micrometer CMOS technology, obtains 1.5 µV residual offset with 2V_{PP} fully differential range. The resolution is 19 bit obtained with 512 clock periods [6]. Another incremental ADC described as low power 22 bits incremental ADC, which include on chip digital filter and low noise or low drift oscillator, realize 0.6-µm CMOS process. It includes a novel fractal sequence-based offset cancellation mechanism, a novel high-accuracy gain control circuit, and a novel reduced-complexity sinc filter realisation. The measured DC offset 2 µV, output noise was 0.25 ppm, INL 4 ppm and gain error 2 ppm. The proposed design with measurement results operates with single 2.7 5 V supply. The total current is 120 microampere during conversion[7].

This paper proposed a9th order delta-sigma modulator with four-bit quantizer to achieve resolution of 24-bit at oversampling ration of 64. The modulator implements topology of cascade of integrators with multiple feedback (CIFB) for higher stability as loop filter order is increased and out-of-band gain (OBG) adjusted to 6. The signal transfer function is flat at low frequencies while noise transfer function shows noise shaping at high frequencies. Also, Noise transfer function with zero optimization technique implemented considering further in-band noise reduction. The integrators inside the loop filter optimized for higher performance. The operational amplifier DC gain, slew-rate as well as unity gain bandwidth also studied. The limited DC gain causes reduction of resolution of the modulator. While the limited slew rate also causes harmonic distortion in signal

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After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the nine-order with 4-bit quantizer for switched-capacitor implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

The design of delta-sigma modulator initiated using modeling of the modulator [8]-[9]. A higher order with nine integrators in the loop filter and four-bit quantizer modulator modeled using Delta-Sigma Toolbox [10]. The CIFF as well as CIFB investigate for higher out-of-band-gain (OBG) of 6 with moderate oversampling ratio of 64 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 148 dB with OSR of 64. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency.. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [9]. Then these

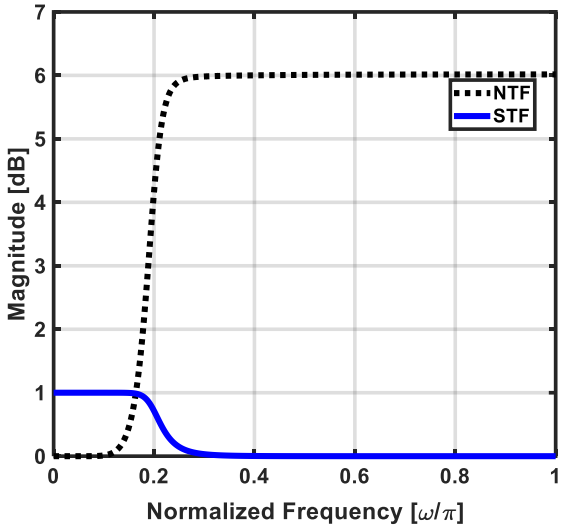

Figure 1: STF and NTF plot (CIFB)

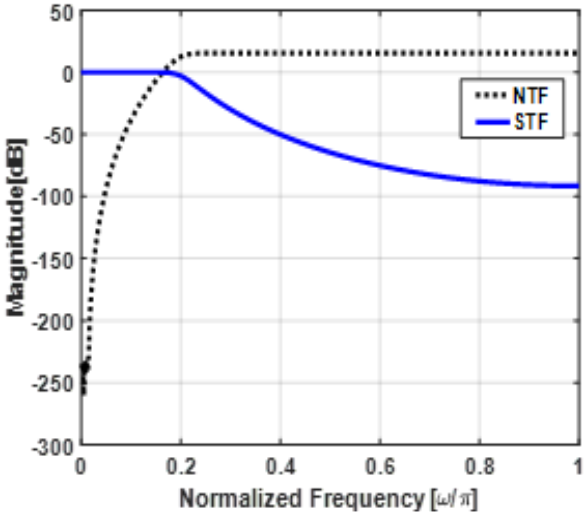

Figure 2: STF and NTF plot (CIFB)

converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero. The signal transfer function and noise transfer function of modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 6. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and

attenuate high frequency signal. The Figure 2 shows ideal STF and Noise transfer function plot of the CIFB modulator topology. The Figure 3 shows the output PSD plot with SNR of 148, achieving effective number of bit (ENOB) of 24-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of -170dB, the quantization noise is suppressed maximum with nine integrators inside the loop filter. Due to moderate OSR of 64, the signal bandwidth is small. Due to CIFB topology of the modulator the signal swing inside the

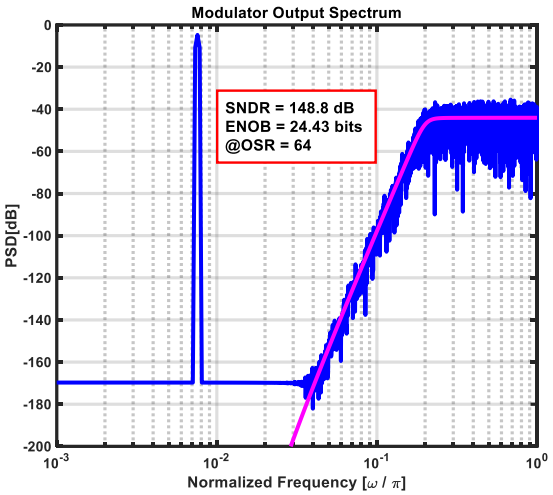

Figure 3: Output PSD plot (CIFB)

loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Because of CIFB topology stability of loop filter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loop filter.

3. RESULTS & DICUSSION

The complete modulator with coefficient obtained from the Toolbox are simulated further to get an estimate the performance of the modulator. To realize the practical implementation of the modulator, non-idealities needs to be simulated so that circuit designed can get an estimate of the performance. The simulation environment SDToolbox [11] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A 9th order delta-sigma modulator with four-bit quantizer to achieve resolution of 24-bit at oversampling ration of 64. The modulator implements topology of cascade of integrators with multiple feedback (CIFB) for higher stability as loop filter order is increased and out-of-band gain (OBG) adjusted to 6. The signal transfer function is flat at low frequencies while noise transfer function shows noise shaping at high frequencies. Also, Noise transfer function zero optimization technique implemented considering further in band noise reduction. The integrators inside the loop filter optimized for higher performance. The operational amplifier DC gain, slew rate as well as unity gain bandwidth also studied. The limited DC gain causes reduction of resolution of the modulator. While the limited slew rate also cause harmonic distortion in signal band. Therefore, it is important to study these performance parameters. As the order of the modulator is higher, the full scale of the modulator will be about 580 mV. Due to multiple feedback topology the signal swing inside the loop filter will be higher. Therefore, it demands

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5. ACKNOWLEDGMENT

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